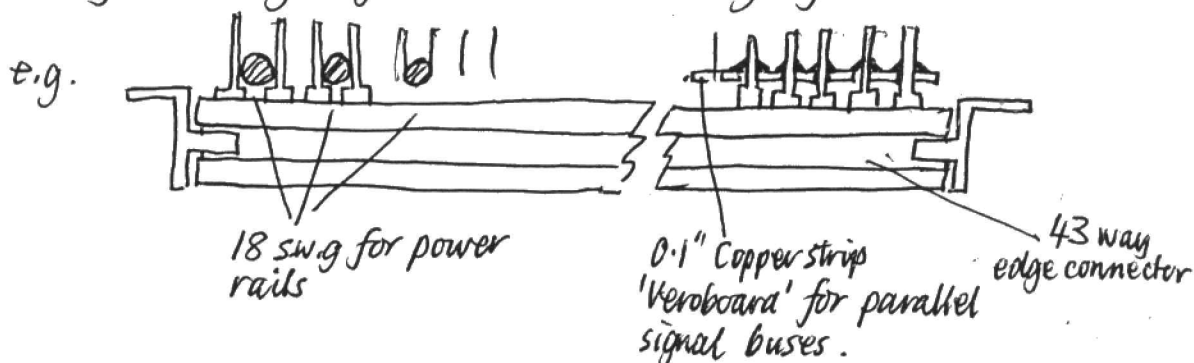


General Remarks regarding board interconnexion, with particular reference to implementing Tiny BASIC V1.2

1. If a standard bus is desired it is suggested that the allocations given on page 15 of our leaflet MP4/2 Sept 1979 (Rev. April 1980) be followed.
2. It is possible to force the majority of the 'Kemitron' boards to conform to the above allocations (i.e. so that any card can go in any slot), if some of the tracks and names of the signals are 'adjusted' (i.e. cut and/or rerouted).
3. An exception to this is the set of VDU A, B, G cards in particular. As they have so many signals unique to just the VDU they cannot be 'adjusted' in this way.
4. We suggest VDU A, B, G be installed as boards 1, 2, 3 and wired point to point e.g. using wire-wrapping techniques. The other cards can be connected using 0.1" strip 'Veroboard' although you may prefer to do all the wiring using discrete pieces of wire, to permit any future modifications and/or extensions to be made.
5. Depending on the size of the system, it is probably best to make the power supply lines from heavy (18 swg.) tinned copper wire, to minimise the voltage dropped along the length of the current carrying conductors.



6. Referring to the remarks on page 15 of our leaflet MP4/2 April 1980, consider carefully whether you want just -5V on the system<sup>bus</sup>, just -12V, or a mixture of the two. The decision affects the wiring on pins 38 and 39 on the bus.
7. An alternative method is to use our 'ISBUS 1.1'. Whilst not intended for the 'Kemitron' range of boards directly (It has provision for 13 double sided, ie. 2x43 way, 0.1" pitch connectors on a completely standardised bus), nevertheless we have found it convenient to build up a system with single sided connectors to run Tiny BASIC Version V1.  
  
The price of this item (which is ~~not yet released~~ <sup>now available</sup>) is ~~expected to be~~ £11.50 ex. handling, tax etc.
8. Note: Even if the 'ISBUS 1.1' mentioned in section (7) above is used it is necessary to make special arrangements for VDU A, B, G, and to some extent DCR-6. Either: leave them off the 'ISBUS' and wire them point to point, or: lift the interconnecting tracks off the relevant 3 or 4 positions and replace with hand wiring.
9. As there is space in the 19" rack generally used, for both a 13-slot 'ISBUS' and a 4" PSU-A assembled module, it is possible to gain extra space for mounting the 'non-ISBUS' VDU A, B, G by moving the ISBUS into the PSU A space and making other arrangements for the power supply. We ourselves have used the ready-made switchmode ASTEC Power Supply which is much smaller than the conventional (non-switching) PSU A, but costs about £30 more, but at least you don't have to wire it.
10. Page 5 of this leaflet is a blank sheet which may help you design your own particular arrangement of boards, page 4 is a similar sheet, which we have filled in with some signal names, and to which we have also added some notes on pushing the boards into a standard (parallel) form to suit our own allocations.

11. Available on request is a sheet we have written called AN-CS/3, 28/5/80. If you are using the 'Kemitron' boards to run Tiny BASIC V1.2, then this lists the various links that should be made to select addresses.
12. Although it involves some modifications to the 'Kemitron' boards to use Tiny BASIC V1.2, there are some particular benefits: Having the VDU on page 'C' and the Keyboard and other I/O on page 'D' leaves space for a good long run of uninterrupted RAM starting on page 1). Although it might be thought better to move the VDU etc even further out of the way, e.g. to page 'E' or 'F' this was not done because many systems using 6800, 6802, 6502 etc generally use 'E' and/or 'F' for their program ROM, and a clash of this nature would inconvenience those brave souls who want to run two different processors on the same bus at the same time.
13. Our 'User Manual' V1.2-UM/2 May 1980 pages 15, 16, 17 gives in the form of 3 Appendices (1, 2, 3) the modifications which are required to the standard 'Kemitron' boards to employ the Tiny BASIC program as its author intended.

The 'User Manual' is supplied free with the pair of firmware chips or separately for 50p (ex handling etc). However we will gladly supply a copy of pages 15, 16, 17 free on request.

D.M.P 27-11-79  
Revised 28-5-80

SLOT 1 IS ON THE LEFT WHEN LOOKING AT FRONT OF RACK (THIS IS BACK VIEW)

PSU A3	TPA 2	SPARE	PP2	MXA3	PRM-8	MZI	DCR-6	VDUG	VDNB	VDUA
-	10	9	8	7	6	5	4	3	2	1
1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6
7	7	7	7	7	7	7	7	7	7	7
8	8	8	8	8	8	8	8	8	8	8
9	9	9	9	9	9	9	9	9	9	9
10	10	10	10	10	10	10	10	10	10	10
11	11	11	11	11	11	11	11	11	11	11
12	12	12	12	12	12	12	12	12	12	12
13	13	13	13	13	13	13	13	13	13	13
14	14	14	14	14	14	14	14	14	14	14
15	15	15	15	15	15	15	15	15	15	15
16	16	16	16	16	16	16	16	16	16	16
17	17	17	17	17	17	17	17	17	17	17
18	18	18	18	18	18	18	18	18	18	18
19	19	19	19	19	19	19	19	19	19	19
20	20	20	20	20	20	20	20	20	20	20
21	21	21	21	21	21	21	21	21	21	21
22	22	22	22	22	22	22	22	22	22	22
23	23	23	23	23	23	23	23	23	23	23
24	24	24	24	24	24	24	24	24	24	24
25	25	25	25	25	25	25	25	25	25	25
26	26	26	26	26	26	26	26	26	26	26
27	27	27	27	27	27	27	27	27	27	27
28	28	28	28	28	28	28	28	28	28	28
29	29	29	29	29	29	29	29	29	29	29
30	30	30	30	30	30	30	30	30	30	30
31	31	31	31	31	31	31	31	31	31	31
32	32	32	32	32	32	32	32	32	32	32
33	33	33	33	33	33	33	33	33	33	33
34	34	34	34	34	34	34	34	34	34	34
35	35	35	35	35	35	35	35	35	35	35
36	36	36	36	36	36	36	36	36	36	36
37	37	37	37	37	37	37	37	37	37	37
38	38	38	38	38	38	38	38	38	38	38
39	39	39	39	39	39	39	39	39	39	39
40	40	40	40	40	40	40	40	40	40	40
41	41	41	41	41	41	41	41	41	41	41
42	42	42	42	42	42	42	42	42	42	42
43	43	43	43	43	43	43	43	43	43	43

32\* involves cutting a track.

Item in brackets ( ) indicates signal on backboard not used.

Blank space indicates uncommitted pin.

So that veroboard can be used as a backplane, the following mods are suggested:

DCR6: Cut track to NADS (PIN 2), Cut tracks to PS 6-φ (PINS 30-36)

Use pins 38-39 for -12v for ASCII KEYBOARD.

Use pin 21 for PS'C' (Page C) for VDM address page select.

MZI IF NIO (PIN 1) and NMRQ (PIN 2) are used, use NMRQ to Enable DCR6, PRM-8, MXA-3, PP2, and "UART Card" (make sure that these cards are DISABLED if NIO (PIN 1) is used for I/O ports.) Some mods may be required on these boards to implement this.

PRM-8 Use an on board regulator to convert -12v to -5v (for safety) (7905+ h/sink)

PP2 Cut tracks to F1 and F2 (PINS 32 and 33) and -50v (PIN 34). Use an on board regulator to convert -12v to -5v (for safety) (7905 no h/sink).

When using IC5 (ie Z80 system) use pins 4,5,6 of IC9 to invert the enable signal IC5 pins 4,12.

SPARE fit a UART to a SPARE card, as described in TINY BASIC V1.1 User Manual to supply and receive RXD and TXD for TPA2 board.

TPA2 Z80's need a UART see "SPARE"



	-	10	9	8	7	6	5	4	3	2	1	
1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6	6
7	7	7	7	7	7	7	7	7	7	7	7	7
8	8	8	8	8	8	8	8	8	8	8	8	8
9	9	9	9	9	9	9	9	9	9	9	9	9
10	10	10	10	10	10	10	10	10	10	10	10	10
11	11	11	11	11	11	11	11	11	11	11	11	11
12	12	12	12	12	12	12	12	12	12	12	12	12
13	13	13	13	13	13	13	13	13	13	13	13	13
14	14	14	14	14	14	14	14	14	14	14	14	14
15	15	15	15	15	15	15	15	15	15	15	15	15
16	16	16	16	16	16	16	16	16	16	16	16	16
17	17	17	17	17	17	17	17	17	17	17	17	17
18	18	18	18	18	18	18	18	18	18	18	18	18
19	19	19	19	19	19	19	19	19	19	19	19	19
20	20	20	20	20	20	20	20	20	20	20	20	20
21	21	21	21	21	21	21	21	21	21	21	21	21
22	22	22	22	22	22	22	22	22	22	22	22	22
23	23	23	23	23	23	23	23	23	23	23	23	23
24	24	24	24	24	24	24	24	24	24	24	24	24
25	25	25	25	25	25	25	25	25	25	25	25	25
26	26	26	26	26	26	26	26	26	26	26	26	26
27	27	27	27	27	27	27	27	27	27	27	27	27
28	28	28	28	28	28	28	28	28	28	28	28	28
29	29	29	29	29	29	29	29	29	29	29	29	29
30	30	30	30	30	30	30	30	30	30	30	30	30
31	31	31	31	31	31	31	31	31	31	31	31	31
32	32	32	32	32	32	32	32	32	32	32	32	32
33	33	33	33	33	33	33	33	33	33	33	33	33
34	34	34	34	34	34	34	34	34	34	34	34	34
35	35	35	35	35	35	35	35	35	35	35	35	35
36	36	36	36	36	36	36	36	36	36	36	36	36
37	37	37	37	37	37	37	37	37	37	37	37	37
38	38	38	38	38	38	38	38	38	38	38	38	38
39	39	39	39	39	39	39	39	39	39	39	39	39
40	40	40	40	40	40	40	40	40	40	40	40	40
41	41	41	41	41	41	41	41	41	41	41	41	41
42	42	42	42	42	42	42	42	42	42	42	42	42
43	43	43	43	43	43	43	43	43	43	43	43	43

Note: Slot 1 is on the left looking at the front. This diagram is a BACK view.

-		10		9		8		7		6		5		4		3		2		1	
1		1		1		1		1		1		1		1		1		1		1	
2		2		2		2		2		2		2		2		2		2		2	
3		3		3		3		3		3		3		3		3		3		3	
4		4		4		4		4		4		4		4		4		4		4	
5		5		5		5		5		5		5		5		5		5		5	
6		6		6		6		6		6		6		6		6		6		6	
7		7		7		7		7		7		7		7		7		7		7	
8		8		8		8		8		8		8		8		8		8		8	
9		9		9		9		9		9		9		9		9		9		9	
10		10		10		10		10		10		10		10		10		10		10	
11		11		11		11		11		11		11		11		11		11		11	
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14		14		14		14		14		14		14		14		14		14		14	
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19		19		19		19		19		19		19		19		19		19		19	
20		20		20		20		20		20		20		20		20		20		20	
21		21		21		21		21		21		21		21		21		21		21	
22		22		22		22		22		22		22		22		22		22		22	
23		23		23		23		23		23		23		23		23		23		23	
24		24		24		24		24		24		24		24		24		24		24	
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26		26		26		26		26		26		26		26		26		26		26	
27		27		27		27		27		27		27		27		27		27		27	
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30		30		30		30		30		30		30		30		30		30		30	
31		31		31		31		31		31		31		31		31		31		31	
32		32		32		32		32		32		32		32		32		32		32	
33		33		33		33		33		33		33		33		33		33		33	
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35		35		35		35		35		35		35		35		35		35		35	
36		36		36		36		36		36		36		36		36		36		36	
37		37		37		37		37		37		37		37		37		37		37	
38		38		38		38		38		38		38		38		38		38		38	
39		39		39		39		39		39		39		39		39		39		39	
40		40		40		40		40		40		40		40		40		40		40	
41		41		41		41		41		41		41		41		41		41		41	
42		42		42		42		42		42		42		42		42		42		42	
43		43		43		43		43		43		43		43		43		43		43	

Note: Slot 1 is on the left looking at the front. This diagram is a BACK view.